FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20853-1E

FLASH MEMORY

CMOS

8M (1M × 8/512K × 16) BIT

MBM29LV800TA-90-X/-12-X/MBM29LV800BA-90-X/-12-X

■ FEATURES

- **Single 3.0 V read, program, and erase**
  Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard world-wide pinouts**
  48-pin TSOP(I) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  44-pin SOP (Package suffix: PF)
  46-pin SON (Package suffix: PN)
  48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  90 ns maximum access time
- **Sector erase architecture**
  One 16K byte, two 8K bytes, one 32K byte, and fifteen 64K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **Data Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/BY)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data in another sector within the same device

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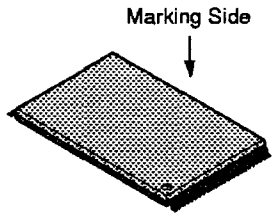
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection Set function by Extended sector protection commandector protection**
- **Temporary sector unprotection**
  Hardware method temporarily enables any combination of sectors from program or erase operations.
- **Extended operating temperature range : –40°C to +85°C**

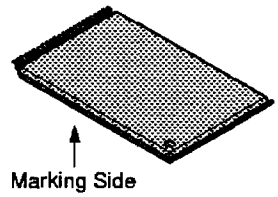
Please refer to "MBM29LV800TA/MBM29LV800BA" in detailed specifications.

■ PACKAGE

48pin-Plastic TSOP(I)

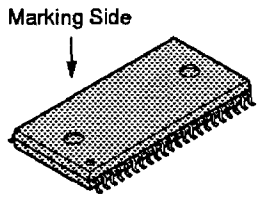


(FPT-48P-M19)



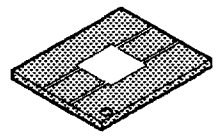
(FPT-48P-M20)

44-pin Plastic SOP



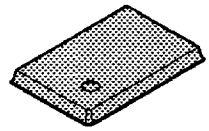
(FPT-44P-M16)

46-pin Plastic SON



(LCC-46P-M02)

48-pin Plastic FBGA



(BGA-48P-M02)

■ GENERAL DESCRIPTION

The MBM29LV800TA-X/BA-X are a 8M-bit, 3.0 V-only Flash memory organized as 1M bytes of 8 bits each or 512K words of 16 bits each. The MBM29LV800TA-X/BA-X are offered in a 48-pin TSOP(I), 44-pin SOP, 46-pin SON, and 48-ball FBGA package. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

The standard MBM29LV800TA-X/BA-X offer access times 90ns, and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29LV800TA-X/BA-X are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29LV800TA-X/BA-X are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

Any sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

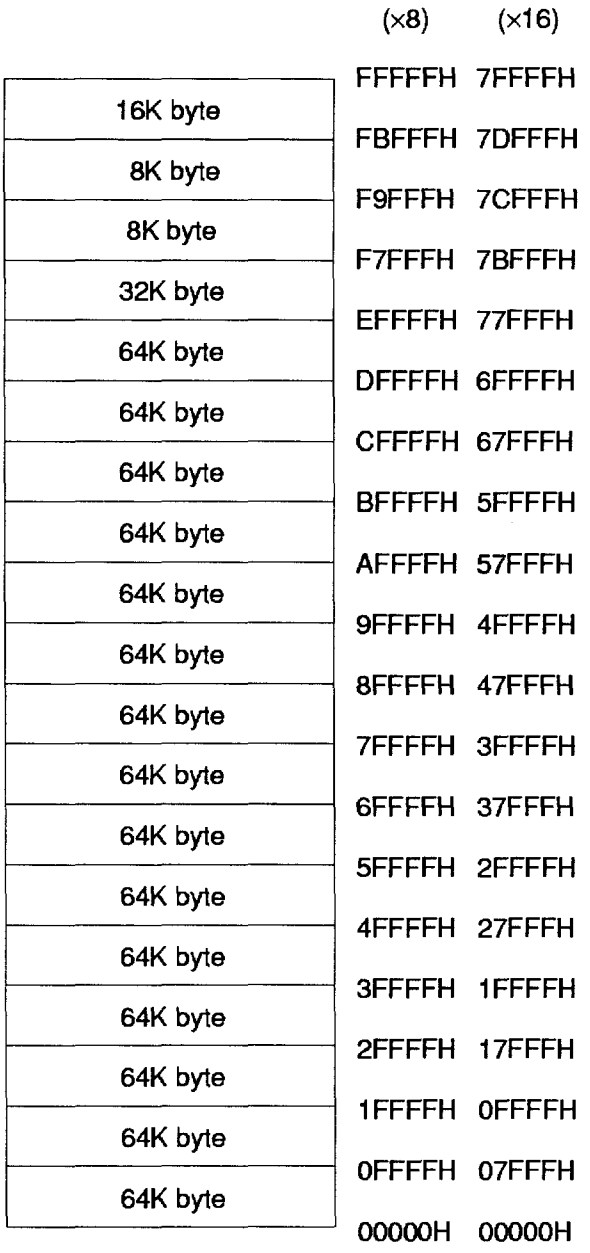
The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29LV800TA-X/BA-X are erased when shipped from the factory.

The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the $RY/\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

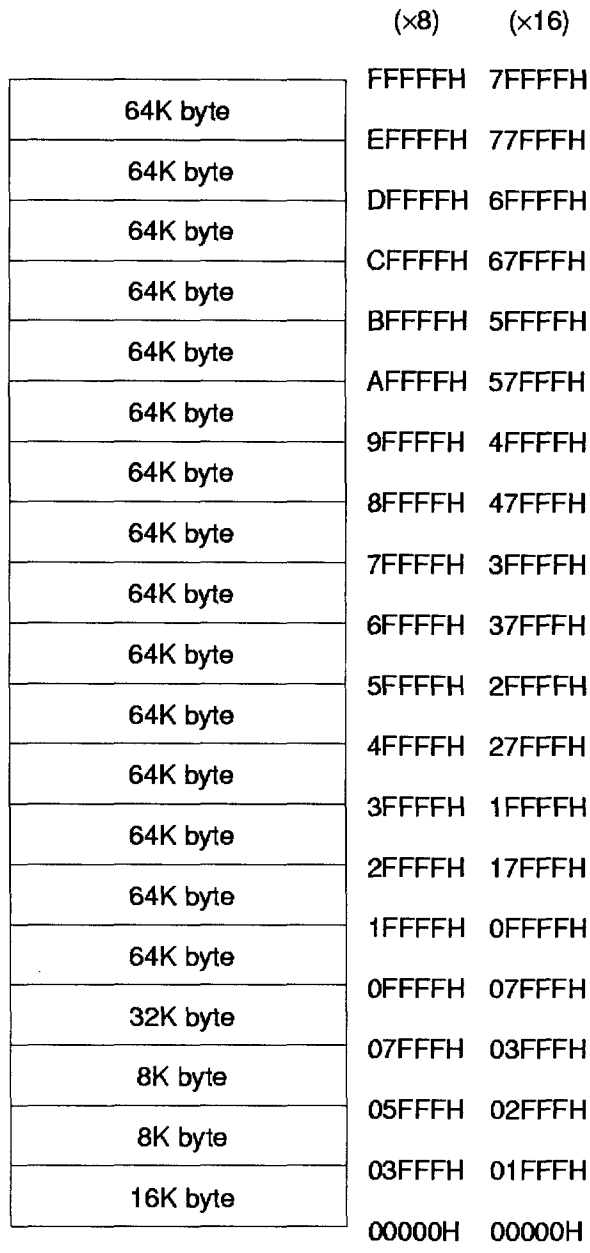
Fujitsu's Flash technology combines years of EPROM and E2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29LV800TA-X/BA-X memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- One 16K byte, two 8K bytes, one 32K byte, and fifteen 64K bytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.



MBM29LV800TA-X Sector Architecture

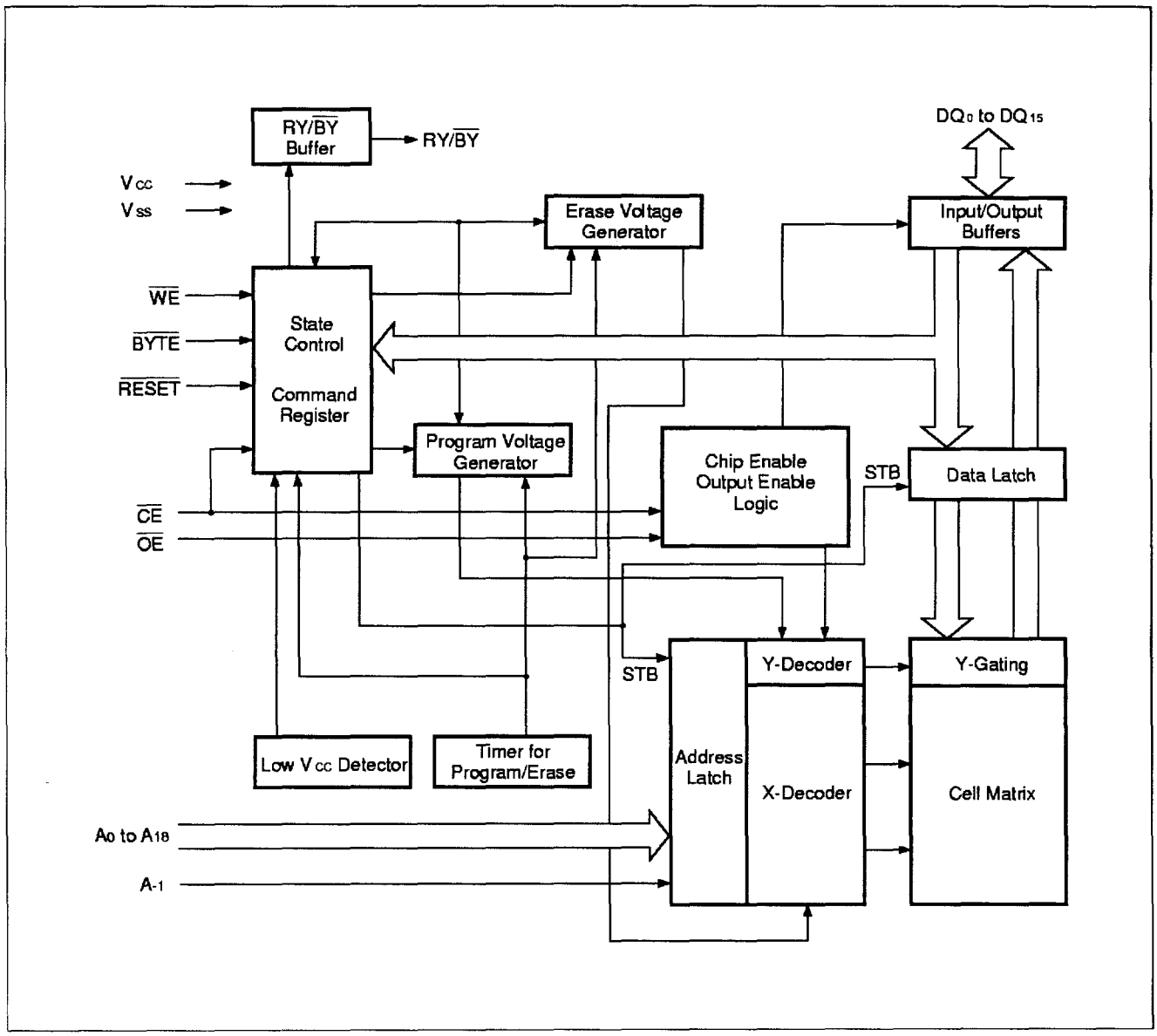


MBM29LV800BA-X Sector Architecture

■ PRODUCT LINE UP

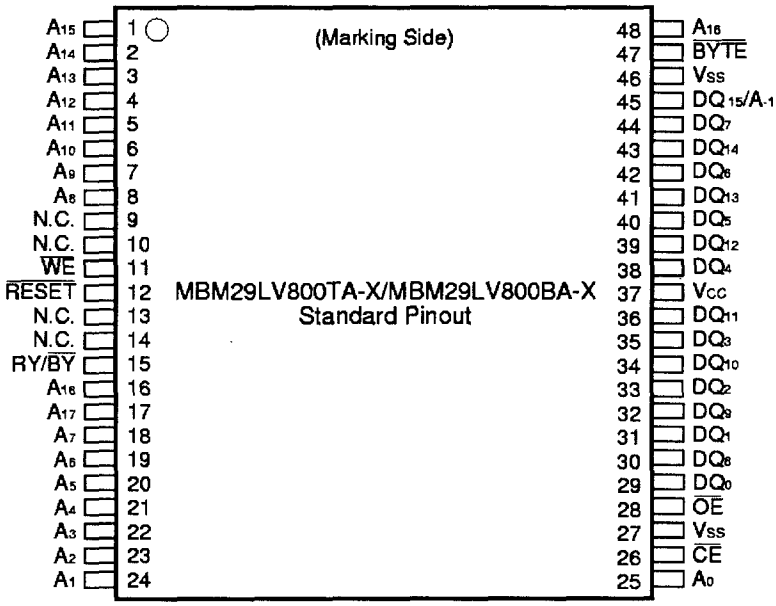
Part No.		MBM29LV800TA-X/MBM29LV800BA-X	
Ordering Part No.	V_{CC} = 3.3 V ±0.3 V	-90	—
	V_{CC} = 3.0 V $^{+0.6\,V}_{-0.3\,V}$	—	-12
Max. Address Access Time (ns)		90	120
Max. $\overline{CE}$ Access Time (ns)		90	120
Max. $\overline{OE}$ Access Time (ns)		35	50

■ BLOCK DIAGRAM

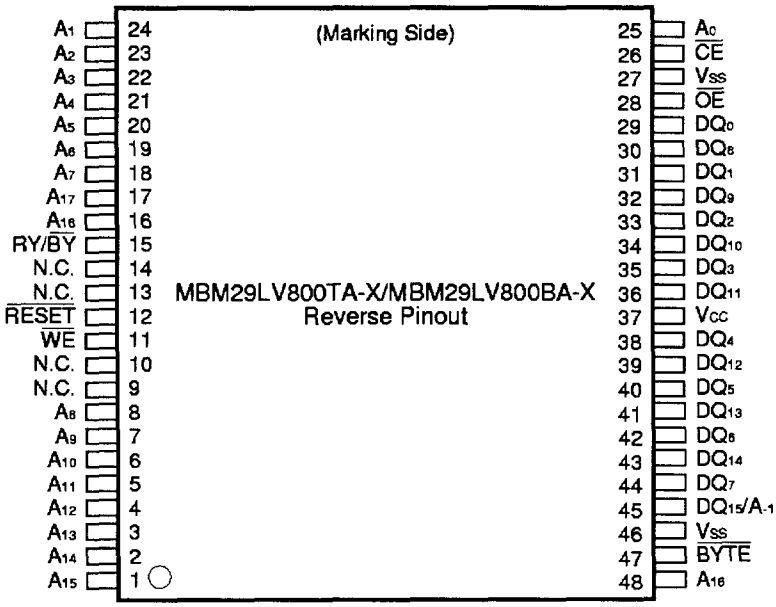


■ CONNECTION DIAGRAMS

TSOP(I)

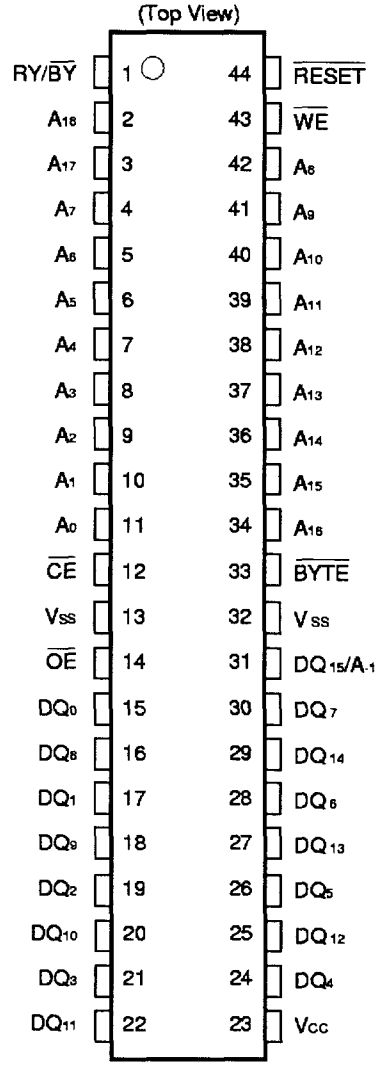


FPT-48P-M19



FPT-48P-M20

SOP
(Top View)



FPT-44P-M16

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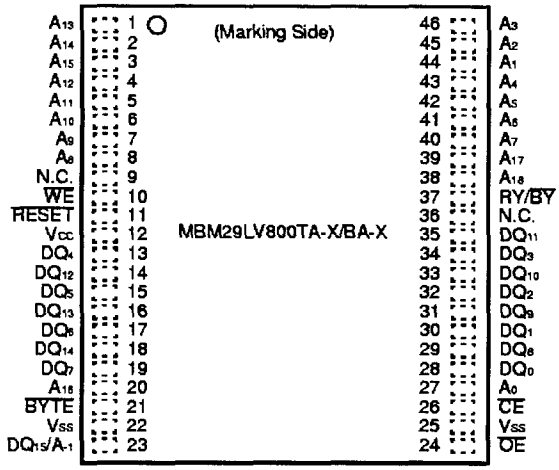
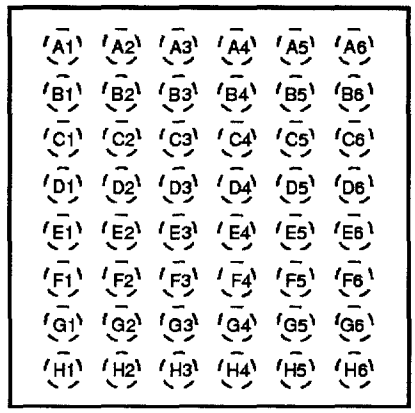
SON
(Top View)



LCC-46P-M02

FBGA
(Top View)
Marking side



BGA-48P-M02

A1	A_3	A2	A_7	A3	RY/$\overline{BY}$	A4	$\overline{WE}$	A5	A_9	A6	A_{13}
B1	A_4	B2	A_{17}	B3	N.C.	B4	$\overline{RESET}$	B5	A_8	B6	A_{12}
C1	A_2	C2	A_6	C3	A_{18}	C4	N.C.	C5	A_{10}	C6	A_{14}
D1	A_1	D2	A_5	D3	N.C.	D4	N.C.	D5	A_{11}	D6	A_{15}
E1	A_0	E2	DQ_0	E3	DQ_2	E4	DQ_5	E5	DQ_7	E6	A_{16}
F1	$\overline{CE}$	F2	DQ_8	F3	DQ_{10}	F4	DQ_{12}	F5	DQ_{14}	F6	$\overline{BYTE}$
G1	$\overline{OE}$	G2	DQ_9	G3	DQ_{11}	G4	V_{CC}	G5	DQ_{13}	G6	DQ_{15}/A_{-1}
H1	V_{SS}	H2	DQ_1	H3	DQ_3	H4	DQ_4	H5	DQ_6	H6	V_{SS}

■ LOGIC SYMBOL

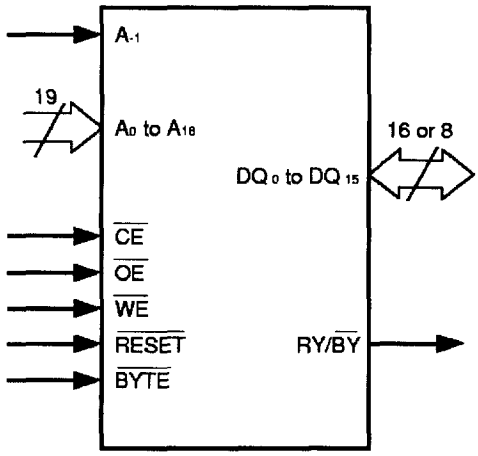


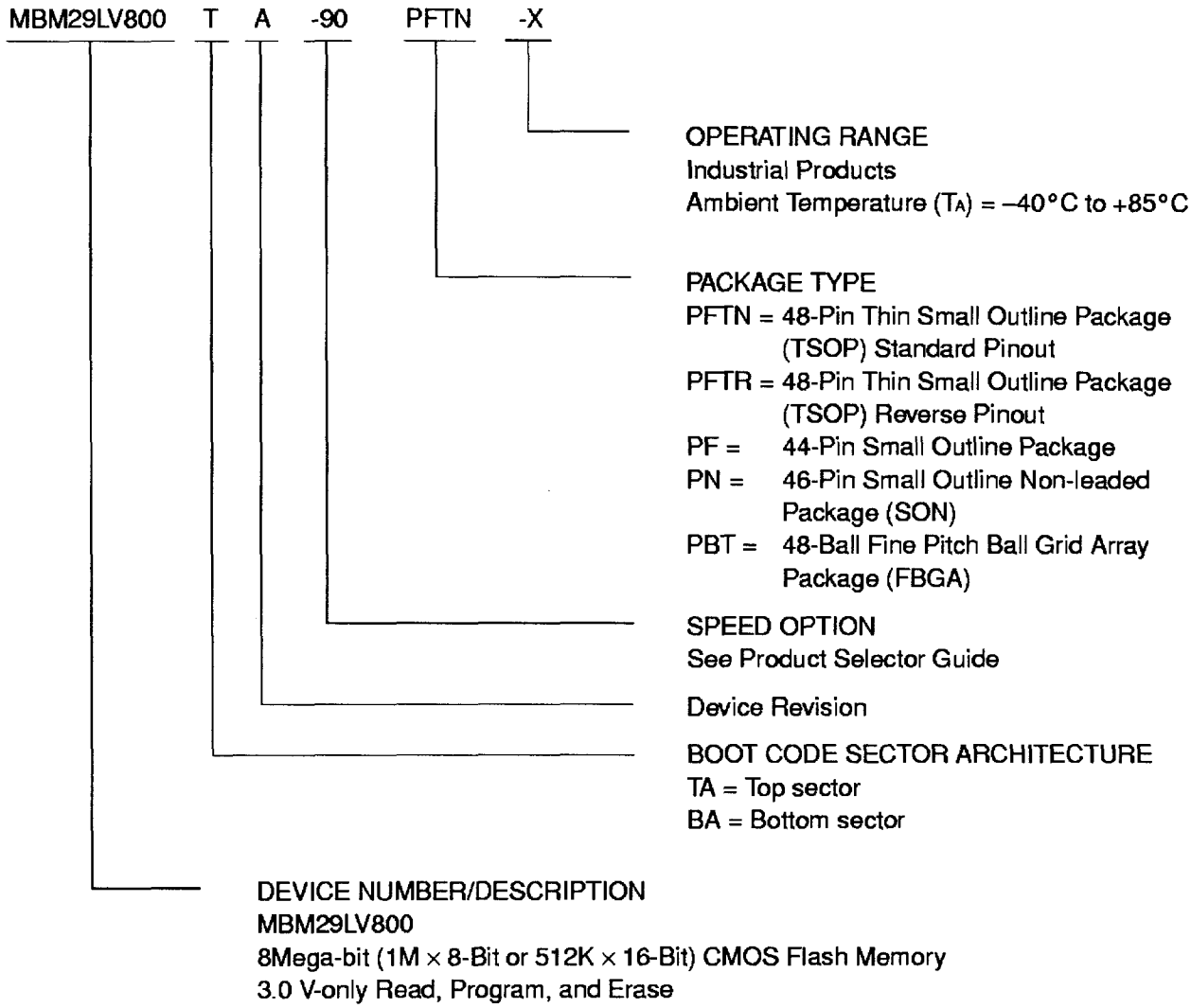
Table 1 MBM29LV800TA-X/800BA-X Pin Configuration

Pin	Function
A_{-1}, A_0 to A_{18}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ ORDERING INFORMATION

Industrial Devices

Fujitsu industrial devices are available in several packages. The order number is formed by a combination of:



■ ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–55°C to +125°C
Ambient Temperature with Power Applied	–40°C to +85°C
Voltage with respect to Ground All pins except A_9, $\overline{OE}$, $\overline{RESET}$ (Note 1)	–0.5 V to V_{CC} + 0.5 V
V_{CC} (Note 1)	–0.5 V to +5.5 V
A_9, $\overline{OE}$, and $\overline{RESET}$ (Note 2)	–0.5 V to +13.0 V

Notes: 1. Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, inputs may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins are V_{CC} +0.5 V. During voltage transitions, outputs may positive overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins are –0.5 V. During voltage transitions, A9, $\overline{OE}$ and $\overline{RESET}$ pins may negative overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins are +13.0 V which may positive overshoot to 14.0 V for periods of up to 20 ns. Voltage difference between input voltage and supply voltage (V_{IN} - V_{CC}) do not exceed 9 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES

Industrial Devices

Ambient Temperature (T_A)	–40°C to +85°C

V_{CC} Supply Voltages

V_{CC} Supply Voltages for MBM29LV800TA/BA-90-X	+3.0 V to +3.6 V
V_{CC} Supply Voltages for MBM29LV800TA/BA-12-X	+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ MAXIMUM OVERSHOOT

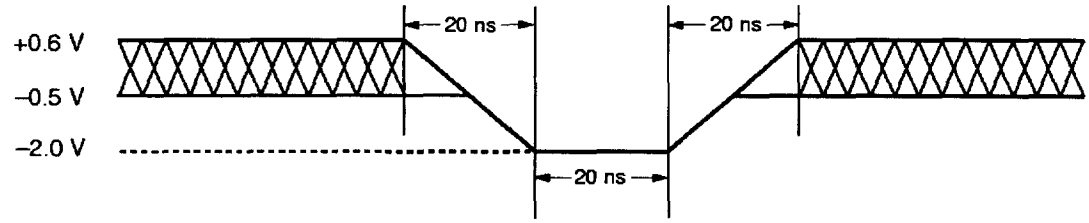


Figure 1 Maximum Negative Overshoot Waveform

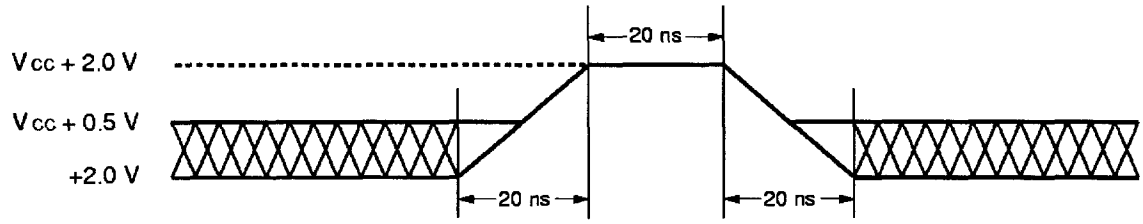
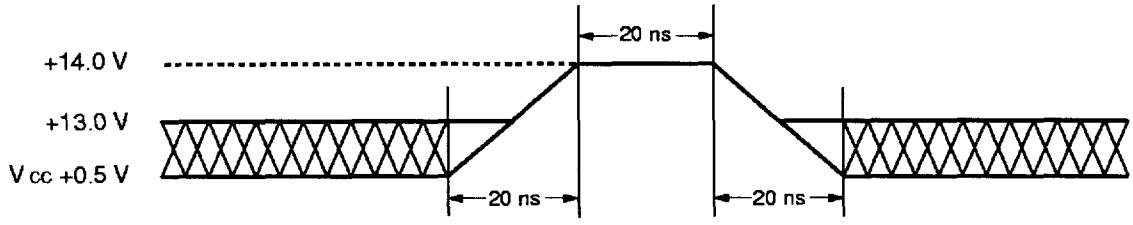


Figure 2 Maximum Positive Overshoot Waveform



*: This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Positive Overshoot Waveform

■ DC CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = Vss to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = Vss to V_{CC}, V_{CC} = V_{CC} Max.		–1.0	+1.0	µA
I_{LIT}	A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	V_{CC} = V_{CC} Max. A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	80	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f=10 MHz	Byte	—	22	mA
			Word		25	
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f=5 MHz	Byte	—	12	mA
			Word		15	
I_{CC2}	V_{CC} Active Current (Note 2)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	35	mA
I_{CC3}	V_{CC} Current (Standby)	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{CC} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V		—	5	µA
I_{CC4}	V_{CC} Current (Standby, Reset)	V_{CC} = V_{CC} Max., $\overline{RESET}$ = Vss ± 0.3 V		—	5	µA
I_{CC5}	V_{CC} Current (Automatic Sleep Mode) (Note 3)	V_{CC} = V_{CC} Max., $\overline{CE}$ = Vss ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V V_{IN} = V_{CC} ± 0.3 V or Vss ± 0.3 V		—	5	µA
V_{IL}	Input Low Level	—		–0.5	0.6	V
V_{IH}	Input High Level	—		2.0	V_{CC}+0.3	V
V_{ID}	Voltage for Autoselect, Sector Protection,and Temporary Sector Unprotection (A_9, $\overline{OE}$, $\overline{RESET}$) (Note 4)	—		11.5	12.5	V
V_{OL}	Output Low Voltage Level	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min.		—	0.45	V
V_{OH1}	Output High Voltage Level	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min.		2.4	—	V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.		V_{CC}–0.4	—	V
V_{LKO}	Low V_{CC} Lock-Out Voltage	—		2.3	2.5	V

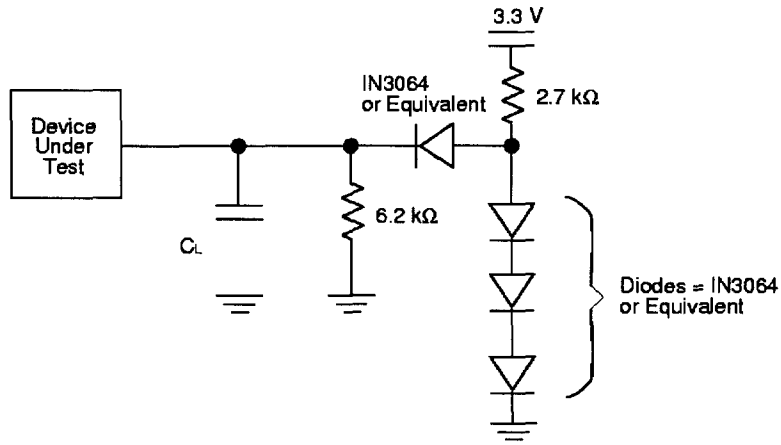
Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 10 MHz).
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. (V_{ID} - V_{CC}) do not exceed 9 V.

■ AC CHARACTERISTICS

• Read Only Operations Characteristics

Parameter Symbols		Description	Test Setup		-90-X (Note)	-12-X (Note)	Unit
JEDEC	Standard						
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max.	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max.	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	35	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	Max.	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	Max.	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	—	Min.	0	0	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	Max.	20	20	µs
—	t_{ELFL} t_{ELFH}	$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	Max.	5	5	ns

Note: Test Conditions:
Output Load: 1 TTL gate and 30 pF (MBM29LV800TA/BA-90-X)
1 TTL gate and 100 pF (MBM29LV800TA/BA-12-X)
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output:1.5 V



Notes: C_L = 30 pF including jig capacitance (MBM29LV800TA/BA-90-X)
C_L = 100 pF including jig capacitance (MBM29LV800TA/BA-10-X/-12-X)

Figure 4 Test Conditions

• **Write/Erase/Program Operations**

Parameter Symbols		Description			-90-X	-12-X	Unit
JEDEC	Standard						
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	0	ns
—	t_{OES}	Output Enable Setup Time		Min.	0	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling	Min.	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min.	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min.	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min.	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	45	50	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min.	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	25	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min.	25	30	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ.	8	8	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		Typ.	1	1	sec
—	t_{VCS}	V_{CC} Setup Time		Min.	50	50	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		Min.	500	500	ns
—	t_{VLHT}	Voltage Transition Time (Note 2)		Min.	4	4	µs
—	t_{WPP}	Write Pulse Width (Note 2)		Min.	100	100	µs
—	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Note 2)		Min.	4	4	µs
—	t_{RB}	Recover Time From RY/$\overline{BY}$		Min.	0	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	500	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		Min.	50	50	ns

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Parameter Symbols		Description		-90-X	-12-X	Unit
JEDEC	Standard					
—	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High-Z	Max.	30	40	ns
—	t_{FHQV}	$\overline{BYTE}$ Switching High to Output Active	Min.	30	40	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	Max.	90	90	ns
—	t_{EOE}	Delay Time from Embedded Output Enable	Max.	90	120	ns

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	1	15	sec	Excludes programming time prior to erasure
Word Programming Time	—	16	5200	µs	Excludes system-level overhead
Byte Programming Time	—	8	3600	µs	
Chip Programming Time	—	8.4	50	sec	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycles	—

■ TSOP(I) PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ SON PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	7.5	9.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	10	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	10	13	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ FBGA PIN CAPACITANCE

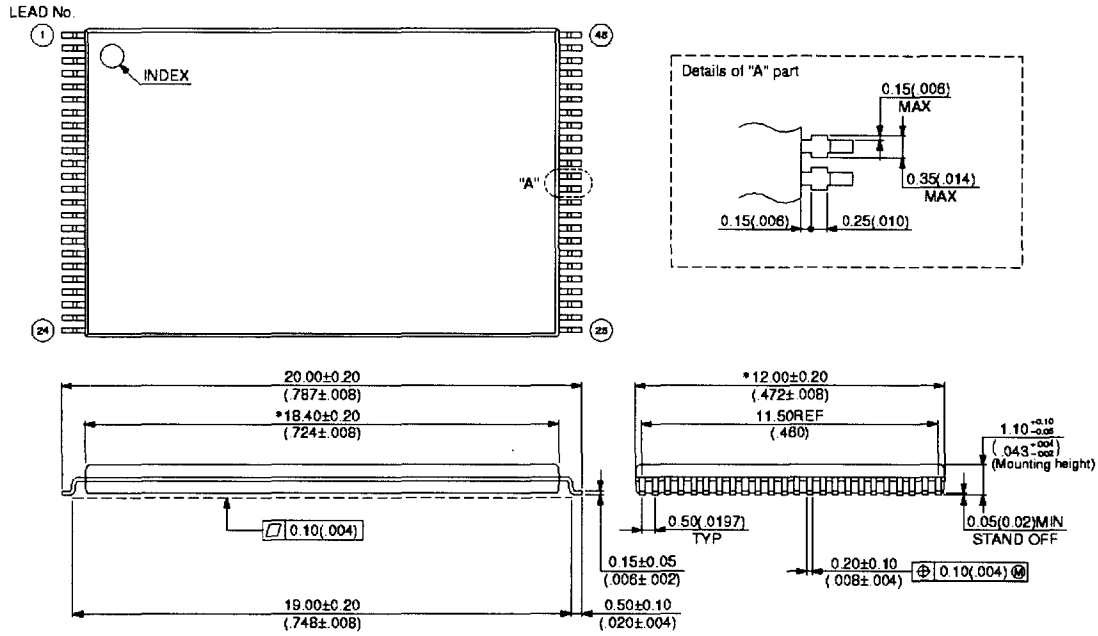
Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	T.B.D.	T.B.D.	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	T.B.D.	T.B.D.	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	T.B.D.	T.B.D.	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(I)
(FPT-48P-M19)

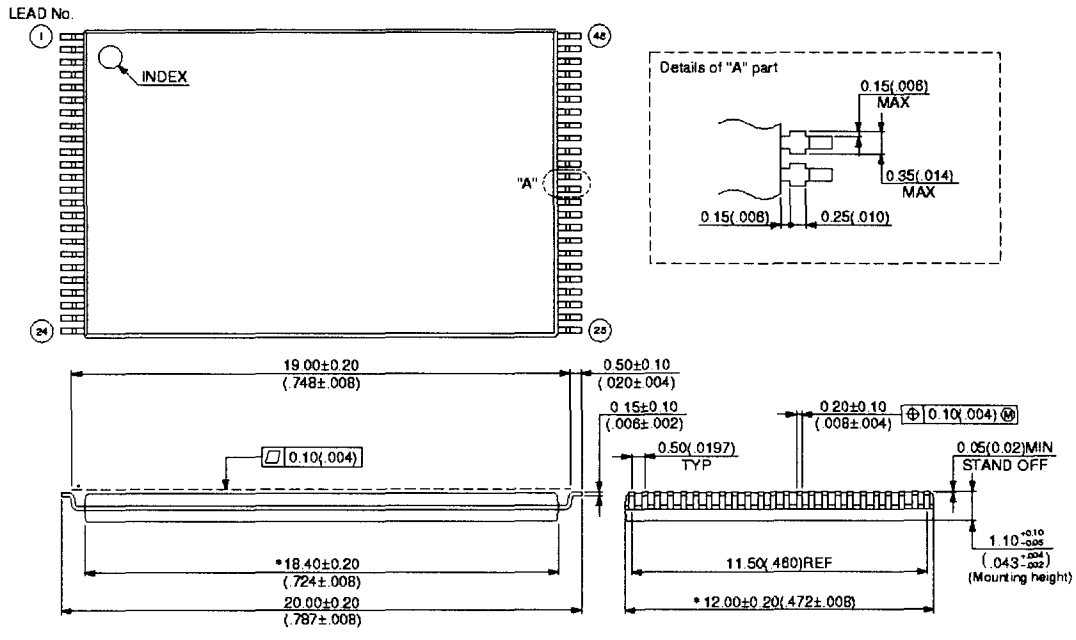
* Resin Protrusin. (Each Side: 0.15 (.006)Max)



Dimensions in mm (inches)

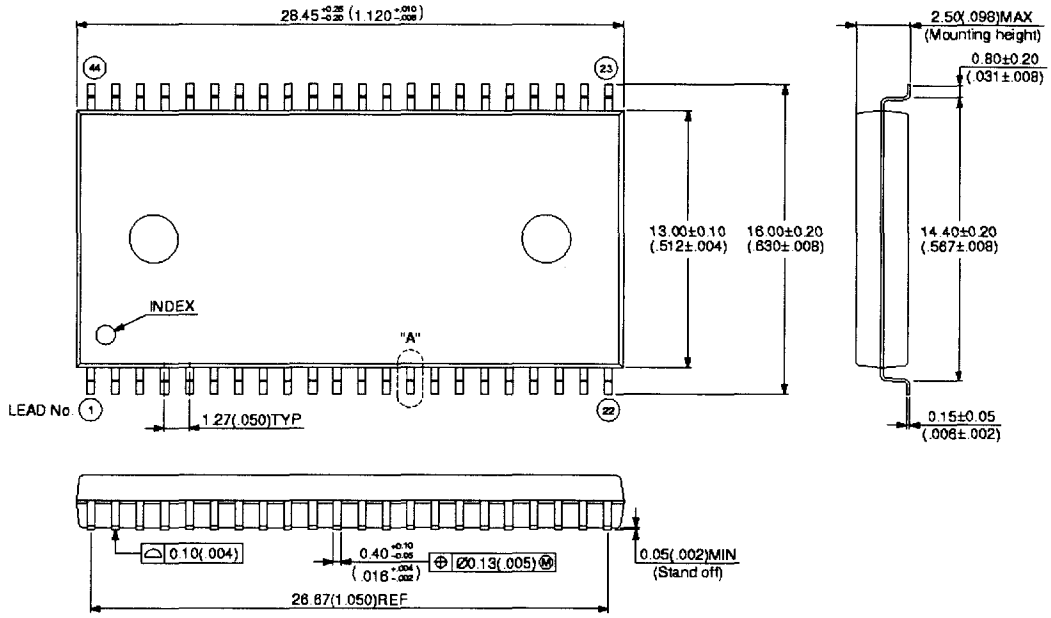
48-pin plastic TSOP(I)
(FPT-48P-M20)

* Resin Protrusin. (Each Side: 0.15 (.006)Max)



Dimensions in mm (inches)

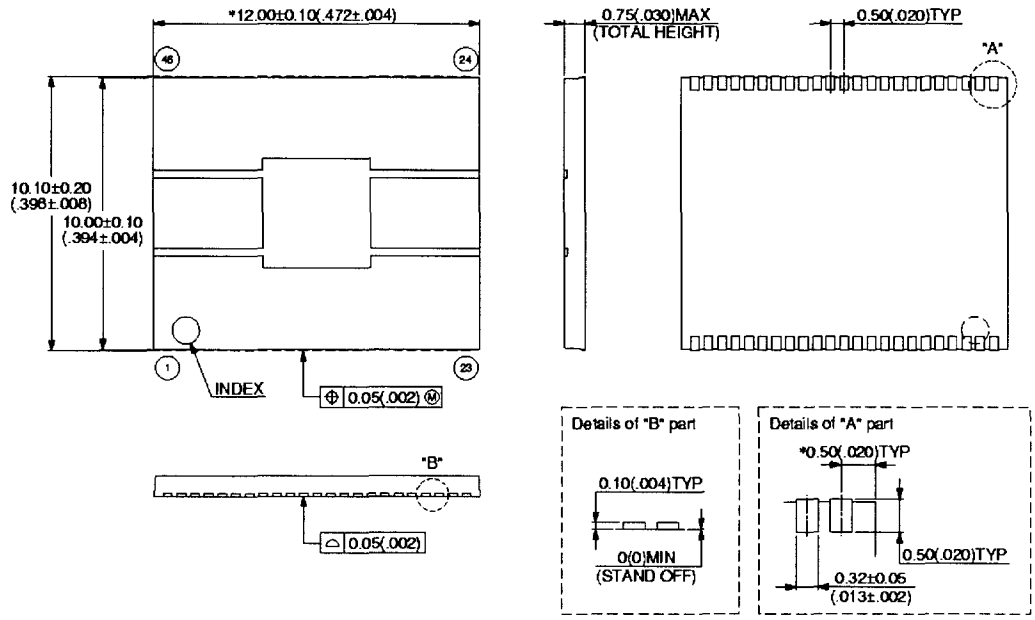
44-pin plastic SOP
(FPT-44P-M16)



Dimensions in mm (inches)

46-pin plastic SON
(LCC-46P-M02)

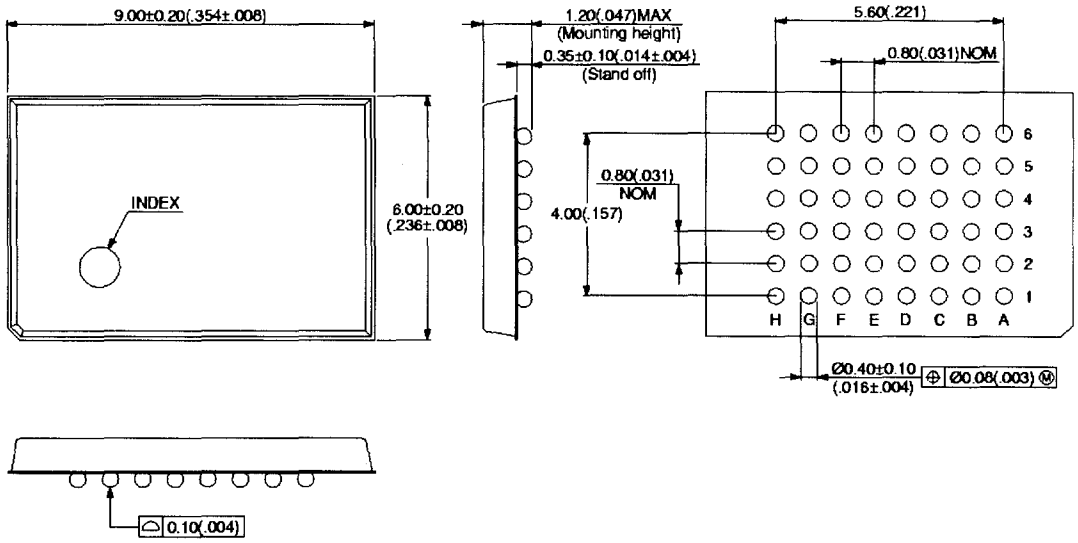
Note 1) Resin residue for * marked dimensions is 0.15 max on a single side.
Note 2) Die pad geometry may change with the models.



Dimensions in mm (inches)

48-pin plastic FBGA
(BGA-48P-M02)

Note: The actual shape of corners may differ from the dimension.



Dimensions in mm (inches)

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